IN THE DRAWINGS

Please replace original FIGs. 2, 3, 5, 6, 8 and 11 with amended FIGs. 2, 3, 5, 6, 8 and 11, contained in the 5 attached Replacement Sheets.

Attachment: 5 Replacement Sheets

REMARKS

Claims 1-18 and 23-26 remain pending in the instant application (hereinafter, the '178 Application). Claims 1, 10 and 11 are amended to improve antecedence and consistency of terminology, and to correct typographical errors. Claim 15 is likewise amended to correct typographical errors, and also to clarify interrelationship of claim features. Claim 23 is amended to improve consistency of claim terminology.

The specification is amended to correct typographical errors and for clarity. In addition, the title is amended in accordance with the Examiner's objection thereto. The specification and the drawings are amended to better correlate the different drawings with each other, per the Examiner's helpful suggestion. Further, paragraph [0047] of the specification and FIG. 11 are amended to change numbering of load 904 to load 962 to remove duplication of element label 904. No new matter is added with the amendments to the claims, the specification or drawings.

It is believed that the following remarks and the above-presented amendments attend to all issues presented in the Office Action dated 21 March 2006. Headings used herein below reflect the order of issues presented in the aforementioned Office Action.

1. Affirmation of Claim Election

We acknowledge the verbal election of Group I claims 1-18 and 23-26, directed to a current mode control system.

2. Drawing Objections

The Examiner has objected to the drawings under 37 C.F.R. 1.83(a). In particular, the Examiner states that the following features must be shown, or cancelled from the corresponding claim:

(**a**) the current controller comprising a positive power FET and a negative power FET (claim 3);

(**b**) the differential current sensor comprising first and second positive reference FETs (claim 4);

(**c**) the differential current sensor comprising first and second negative reference FETs (claim 5);

(**d**) the positive power FET comprising XFETs substantially identical to the first positive and negative reference FETs (claim 6);

(e) X equaling 40,000 (as in claims 7 *and* 9)

(f) the negative power FET comprising X FETs substantially identical to the second positive and negative reference FETs (claim 8);

(g) the differential current sensor comprising a first comparator (claim 10);

(h) the differential current sensor comprising a second comparator (claim 11);

(i) the system comprising a driver (claim 12)

(j) the offset signal generated from a reference source within the system (claim 14);

(k) the differential current sensor comprising first, second and third transistors, first and second current sources, and a differential amplifier (claim 15).

The Examiner notes that many of the objections could be probably be corrected by properly correlating the different drawings with one another. Accordingly, the specification and drawings are amended to correlate the drawings. In particular, the drawings and specification are amended to reference system 100 (in accordance with the system described in the remaining pending claims), to cross-reference different embodiments of the same feature, and to reflect the language utilized in the claims. These amendments address each of items (a)–(k), as follows:

- Feature (a) is supported by amended FIG. 8, now including a dotted box representing switch 520.
- Features (b) and (c) are also supported by amended FIG. 8, and by the amendment to paragraph [0035], above. These amendments illustrate that sensing elements 602, 604 may be included with differential current sensor 28. As shown and described, combined sensing elements 602, 604 include positive FETs 610, 614 and negative FETs 612, 616.
- Features (d) - (f) are also supported by amended FIG. 8, in particular, by the replacement of capitalized or lower case M's (in "MREF NEG," "MREF POS," XOUT NFET," XOUT PFET," "m=1," and "m=40,000") with X's. The drawings now show the positive power FET comprising X FETs substantially identical to the first and second positive reference FETs (as in claim 6). Amended FIG. 8 also shows the negative power FET comprising X FETs substantially identical to the first and second negative reference FETs (as in claim 8,). X= 40,000 (as in claims 7 and 9) is also depicted in amended FIG. 8.

- Features (**g**) and (**h**) are resolved given the amendments to claims 10 and 11 which clarify that the current controller comprises the features formerly ascribed to the differential current sensor.
- Features (**i**) is supported by the addition of reference number 22 in a manner indicating that switching current amplifier 128B may be interchangeable with switching current amplifier 22. This serves to relate the following elements, described in claim 11, base claim 1 and intervening claims: the driver with a current amplifier; first and second comparators; a switch; a differential current sensor with first and second neg reference FETs and first and second positive reference FETs; a current controller with a positive FET and a negative FET, and an error amplifier. This amendment is supported at least by the recitation that "Figure 8 is a schematic diagram illustrating one embodiment of a switching current amplifier 126B suitable for use as switching current amplifier 22, figure 6," Specification, [0035].
- Feature (**j**) is supported by amended FIG. 11 and the corresponding amendments to the Specification (see amended ¶ [0032], above), which now include reference number 919 to indicate a reference source within the system. Support for this amendment is found in paragraph [0032] of the specification which discloses that the reference voltage VBG is a bandgap voltage with an exemplary value of 1.23V. Of note, the use of bandgap techniques for reference voltage generation is well known in the art.
- The issue regarding feature (**k**) is resolved with the amendment to claim 15. Amended claim 15 requires a differential current sensor comprising a differential current threshold detector, comprising a first transistor and a second transistor that couple to various elements (recited in the claim). Such a differential current sensor is shown, for example, in FIG. 8.

3. Title

The title of the instant application is amended to "System and Method for Controlling an Output Voltage Across a Load" in accordance with the Examiner's requirement. The new title clearly indicates the inventions to which the claims are directed.

4. Claim Objections

The Examiner objects to claims 1-18 and 23-26 because claims 1 and 23 recite "an average current." Claims 1 and 23 are amended to recite "the desired average current", in accordance with the Examiner's requirement.

5-7. Claim Rejections – 35 U.S.C. § 102

Given the cancellation of claims noted herein, claims 1, 18, 23 and 26 stand rejected as being anticipated by U.S. Patent No. 5,912,552 (hereinafter, "Tateishi"). Respectfully, we disagree.

As way of background, the '178 Application teaches of a system and method that directly controls the average current through a load by controlling both the positive and negative peak currents. Controlling both positive and negative peak current is important because changes in input voltage, output voltage, inductance of Lout, switching frequency, etc., will not change the relationship between the peak and average current. Current through inductor Lout (e.g., inductor 910, Figure 11) is sensed by comparing voltage across the power FETs (e.g., PFET 618 and NFET 620, Figure 8) to voltage across a reference FET (e.g., reference FETs 610, 612, 614 and 616). No external sense resistor is required to sense current through the inductor. The switching frequency of the '178 system and method is determined by the inductor slew rates (i.e., di(Lout)/dt, which depends on Vin, Vout and Lout) and the hysteretic current threshold levels. No clock or timer is required to generate or determine the switching frequency. More specifically, the error between the load voltage and the reference voltage is determined by sensing the output current of the error amplifier (e.g., error amplifier 118, Figure 3, 940, Figure 11) and not the output voltage of the error amplifier. The output voltage of the error amplifier is always equal to the voltage applied to VDES 906, Figure 11, which is a filtered version of the reference voltage VREF 912. Resistor RFB 914 is connected between the output of the error amplifier (at pin VFB 904) and the load voltage (SENSE+ Figure 11). Any voltage difference between VFB and SENSE + generates a current through resistor 914 and through the output stage of the error amplifier, and the current is proportional to (VFB-SENSE+)/RFB. This current is sensed at the output of the error amplifier and becomes the error signal which controls the switching of the regulator. Note that the gain of the error signal is easily changed by changing the value of RFB resistor 914. Further, note that changing RFB does not

change the nominal output voltage of the regulator. The gain of the error amplifier is important for at least two reasons. First, the gain of the error amplifier affects the output droop (i.e., how much the load voltage changes versus load current) of the system and method, which is needed to control current sharing between separate regulators. Second, the gain of the error amplifier also affects the transient response of the system to changes in load current by affecting the loop gain and unity-gain bandwidth of the regulator voltage feedback loop. This allows the error gain to be adjusted to suit the needs of different applications.

On the other hand, Tateishi only controls the positive peak current. If only the positive peak current is controlled, changes in the input voltage, output voltage, inductance of Lout, switching frequency, etc., will change the relationship between peak and average current. Tateishi will therefore need to change VCNTL to accommodate any changes in input voltage, output voltage, inductance of Lout, switching frequency, etc., because the average output current must stay the same in order to maintain a fixed output voltage. Tateishi senses output current using a sense resistor in series with the inductor. The switching frequency of Tateishi is determined either by an oscillator/clock or a one-shot timer. Tateishi uses an error amplifier with a very high input impedance to compare a fraction of the load voltage to a reference voltage; the error amplifier generates an output voltage (VCNTL) proportional to the error between the fractional load voltage and the reference voltage. In Tateishi, the gain of the error signal is determined by the gain of the error amplifier (labeled 58 in Figure 5 of the Tateishi patent) and not by the resistors R1 and R2. The purpose of R1 and R2 is to divide down the load voltage so that it can be compared with the reference voltage. Changing R1 and/or R2 will change the divider ratio and, therefore, change the nominal output voltage of the regulator. Tateishi is not flexible and does not allow the error gain to be adjusted to suit the needs of different applications.

Tateishi

To anticipate a claim, Tateishi must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." MPEP 2131 citing *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and *Richardson v. Suzuki Motor* Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989). However, Tateishi does not teach or suggest every

element in Applicant's claims 1, 18, 23, 24 and 26. We therefore respectfully disagree with and traverse the Examiner's rejection, for at least the following reasons:

Claim 1: Amended claim 1 recites a system for controlling an output voltage across a load using current mode control to control current through an output filter connected to the load, including:

a) an error amplifier for generating a reference current signal indicative of a desired average current through the load by comparing a voltage across the load to a reference voltage.
b) a differential current sensor having hysteresis that uses the reference current signal to generate a control signal indicating when an output current is greater than the desired average current; and
c) a current controller, responsive to the control signal to alternately couple the output filter to a first supply rail and to a second supply rail, to generate the desired average current through the load.

Tateishi does not disclose an error amplifier for generating a reference current signal indicative of a desired average current through the load by comparing a voltage across the load to a reference voltage, as in element (a). Rather, in Tateishi, error amplifier 58 compares voltages V_{FB} to V_{REF} to generate a first feedback signal that is a voltage reference used as input to comparators 56 and 60. See Tateishi col. 6, lines 55-57. This first feedback signal is not a reference current signal. In addition, the reference signal (V_{CTRL}) referenced by the Examiner is not indicative of a desired average current as asserted (i.e., there is no way to determine what the desired average current is at any moment, by looking at just the Vctrl signal). Tateishi, col. 6, lines 53-54, specifically discloses that the V_{CTRL} signal represents the target peak inductor current for the regulated voltage.

As to claim 1 element (b), as noted above, Tateishi does not teach or disclose a reference signal indicating average current since Tateishi's V_{CTRL} represents the target peak inductor current. Tateishi cannot and does not, therefore, disclose a differential current sensor having hysteresis that uses the reference current signal to generate a control signal indicating when an output current is greater than the desired average current.

In addition, since Tateishi fails to teach or suggest a reference signal indicative of the desired average current, Tateishi can not and does not use such a reference signal

to alternately couple the output filter to first and second supply rails, as recited in element (c) of claim 1.

Because Tateishi does not teach or suggest every element of claim 1, there is no anticipation. We respectfully request withdrawal of the rejection.

Claim 18: Claim 18 depends from claim 1, and further recites an external resistor connected between the load and the error amplifier, for determining the output voltage droop. Contrary to the Examiner's note, Tateishi does not disclose this limitation. Although Tateishi's V_{FB} is a feedback voltage representative of the output voltage, Tateishi makes no disclosure of utilizing V_{FB} to determine or control output voltage droop. Withdrawal of the Examiner's rejection is thus respectfully requested.

Claim 23: Amended claim 23 recites a method for controlling an output voltage across a load, including:

(a) comparing the output voltage across the load to a reference voltage;
(b) generating a reference current signal indicative of a desired average current through the load;
(c) generating a control signal indicating when an output current is greater than the desired average current; and
(d) alternately coupling an output filter to a first supply rail and to a second supply rail in response to the control signal, to generate the desired average current through the load.

As noted above and argued with respect to claim 1, Tateishi fails to disclose a current signal indicative of a desired average current, as required in element (b). It therefore follows that Tateishi also fails to disclose generating a control signal indicating when an output current is greater than the desired average current as required by step (c). Tateishi's mode of operation is based upon a positive peak current. We thus respectfully request withdrawal of the Examiner's rejection.

Claim 26: Claim 26 depends from claim 23, thus benefiting from like argument. Furthermore, claim 23 recites determining a voltage droop via an external resistor connected to the load. As noted, Tateishi does not disclose determining or controlling output voltage droop. Tateishi also fails to disclose external resistors as presented in the context of claim 23.

Umemoto

Given the cancellations made herein, claims 1, 3, 13, 14 and 23 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,815,939 (hereinafter, "Umemoto"). We must again respectfully disagree and traverse these rejections, since Umemoto does not teach every element of the rejected claims.

The operation of Umemoto is similar to Tateishi, and is therefore different to the '178 Application. Umemoto only controls the positive peak current and therefore anything that changes the peak-to-peak current (e.g., changes in input voltage, output voltage, output inductance, switching frequency, etc.) will change the relationship between the peak and average currents. Therefore, to accommodate any of these changes, Umemoto must change Vgm in order to maintain the average output current and output voltage. Umemoto senses the output current using a sense resistor (resistor 15, FIG. 1) in series with the inductor (Lo). The switching frequency of Umemoto is determined by an oscillator/clock. Umemoto uses a mutual-conductance amplifier (16, FIG. 1) with a very high input impedance to compare the load voltage to a reference voltage; this amplifier generates an output voltage (Vgm) proportional to the error between the load voltage and the reference voltage. In Umemoto, the gain of the error signal is determined by the fixed gain of the amplifier (16, FIG. 1); there is no provision within Umemoto for changing the gain of this amplifier (and hence the gain of the error signal) to suit the needs of different applications.

Claim 1: We must respectfully disagree with the Examiner's 102 rejection in view of Umemoto. For example, Umemoto does not disclose an error amplifier for generating a reference current signal indicative of a desired average current through the load by comparing a voltage across the load to a reference voltage, as in element (a). Rather, in Umemoto, amplifier 16 compares voltages Vo to Vref to generate a voltage, Vgm, that is used as input to comparator CP1. See Umemoto col. 3, lines 34-44 and FIG. 1. Voltage Vgm is not a reference current signal. Umemoto is silent as to hysteretic components, as required in claim element (b). Furthermore, Umemoto fails at least to disclose a current controller, responsive to the control signal to alternately couple the output filter to a first supply rail and to a second supply rail, to generate the desired average current through the load, as in claim element (c). For example, Umemoto is silent as to filters. Because Umemoto does not teach every element of claim 1, or show the identical element in as complete detail as in claim 1, Umemoto

fails under 35 U.S.C. § 102. Withdrawal of the Examiner's rejection is therefore requested.

Claims 2, 3, 13 and 14: These claims depend from claim 1, and thus benefit from like argument. However, additional patentable features of claims 2, 3, 13 and 14 include, but are not limited to the following:

Claim 3 requires a current controller having a positive FET that couples and de-couples the output filter to and from the first supply rail, and a negative FET that couples and decouples the output filter to and from the second supply rail. Umemoto does not teach these features, instead requiring two n-type transistors to form a switching circuit. See Umemoto col. 3, lines 15-20 and items 11 and 12, FIG. 1.

Umemoto does not teach an offset signal representative of half an allowable ripple on an output current, as in claim 13.

Claim 14 depends from claim 13 and further requires that the offset signal be generated from a reference source within the system. Since Umemoto does not teach the limitations of claim 13, Umemoto cannot anticipate claim 14.

Claim 23: As noted above with respect to claim 1, Umemoto fails to disclose a current signal indicative of a desired average current, as required in elements (b)-(d). Since Umemoto operates by controlling the peak output current, the signal R of Umemoto represents an indication of whether an output current exceeds a desired peak output current and is not indicative of a desired average current through a load. We thus respectfully request withdrawal of the Examiner's rejection.

Claims 24-25: These claims depend from claim 23, and thus benefit from like argument. Furthermore, as noted above, Umemoto is silent as to hysteretic components as recited by claims 24 and 25. Again, we respectfully request withdrawal of the Examiner's rejections.

8. Allowable Claims

We thank the Examiner for his indication that claims 4-12 and 15-17 would be allowable if rewritten to overcome the claim objection previously addressed, and to incorporate the limitations of the base claim and any intervening claims. We

agree that the subject matter of claims 4-12 and 15-17 is allowable over the art of record.

Conclusion

In view of the above amendments and clarifications, all issues set forth in the pending office action have been addresses and it is believed that claims 1-18 and 23-26 are allowable over Tateishi and Umemoto. We therefore respectfully solicit a notice of allowance.

No fees are believed due; however, if any fee is deemed necessary in connection with this Amendment and Response, please charge Deposit Account No. 12-0600. Should any issues remain outstanding, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully Submitted,

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Curtis A. Vock, Reg. No. 38,356
LATHROP & GAGE, L.C.
4845 Pearl East Circle, Suite 300
Boulder, Colorado 80301
Tel: (720) 931-3011
Fax: (720) 931-3001